

Claim Chart for U.S. Patent No. 8,462,835

<u>U.S. Patent No. 8,462,835</u>	<u>Infringement Allegations</u>
<p>8. An apparatus configurable to adapt forward error correction and interleaver parameter (FIP) settings during steady-state communication or initialization comprising</p>	<p><u>ITU-T G.993.2 VDSL2 Standard</u></p> <p>The Accused Products operate in accordance with the VDSL2 (i.e., ITU-T G.993.2) standard comprise an apparatus configurable to adapt forward error correction and interleaver parameter (FIP) settings during steady-state communication or initialization. See, e.g., ITU-T G.993.2 (12/2011) at § 9.4.1 <i>Dynamic change of interleaver depth</i>:</p> <div style="display: flex; justify-content: space-around; align-items: center;"> <div style="text-align: center;"> <p>ITU-T</p> <p>TELECOMMUNICATION STANDARDIZATION SECTOR OF ITU</p> </div> <div style="text-align: center;"> <p>G.993.2</p> <p>(12/2011)</p> </div> </div> <p>SERIES G: TRANSMISSION SYSTEMS AND MEDIA, DIGITAL SYSTEMS AND NETWORKS</p> <p>Digital sections and digital line system – Access networks</p> <hr/> <p>Very high speed digital subscriber line transceivers 2 (VDSL2)</p>

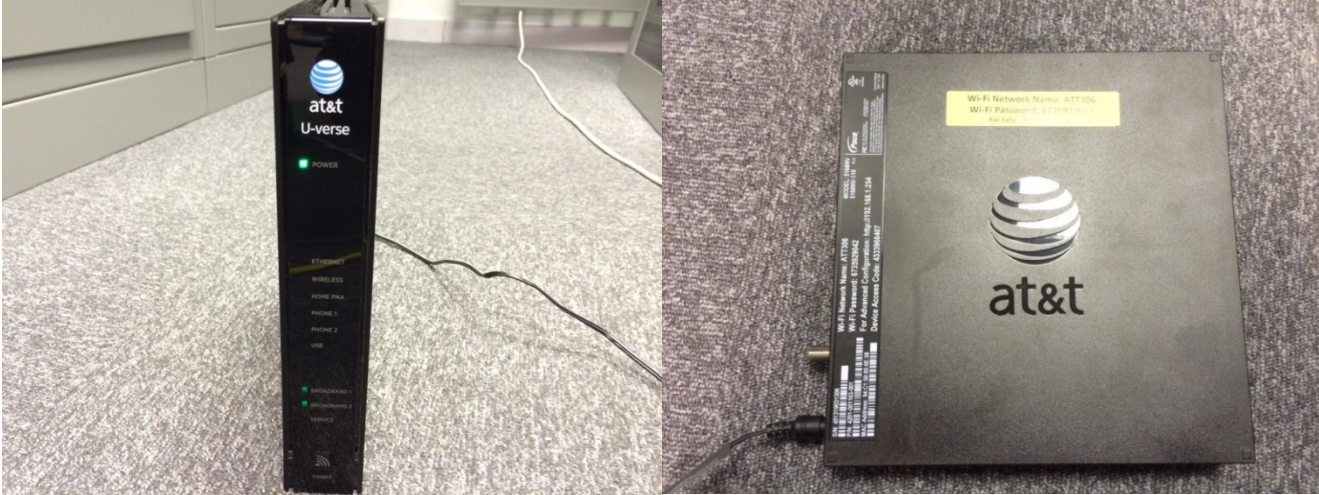
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	<p>Figure 5-4 – Generic application reference model for remote deployment with splitter</p>

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	<p>Recommendation ITU-T G.993.2</p> <p>Very high speed digital subscriber line transceivers 2 (VDSL2)</p> <p>1 Scope</p> <p>This Recommendation is an enhancement to [ITU-T G.993.1] that supports transmission at a bidirectional net data rate (the sum of upstream and downstream rates) up to 200 Mbit/s on twisted pairs. This Recommendation is an access technology that exploits the existing infrastructure of copper wires that were originally deployed for POTS (plain old telephone service).</p> <p>This Recommendation specifies only discrete multi-tone (DMT) modulation and incorporates components from [ITU-T G.993.1] (VDSL), [ITU-T G.992.3] (ADSL2), and [ITU-T G.992.5] (ADSL2 plus).</p> <p>...</p> <p>For PMS-TC sublayer specifically, changes in this Recommendation relative to [ITU-T G.993.1] include:</p> <ul style="list-style-type: none"> • Improved framing (based on [ITU-T G.992.3]); • The definition of two latency paths and two bearer channels; • Improved OLR mechanisms (based on [ITU-T G.992.3]), including optional SRA, SOS, and dynamic interleaver change; <p>9.4.1 Dynamic change of interleaver depth</p> <p>A method to dynamically change the interleaver depth during transmission is defined for VDSL2. This method is optional. Support shall be indicated during initialization in O-MSG 1 and R-MSG 2.</p> <p><i>See also, e.g., ITU-T G.993.2 (02/2019 at § 9.4.1 Dynamic change of interleaver depth:</i></p> <p><u>Testing</u></p>

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	<p>Testing was performed on the Pace 5168NV.</p> <div data-bbox="340 310 1650 802">  </div> <p>Testing was performed on the Pace 5168NV connected to an Alcatel/Nokia ISAM 7330 DSLAM using a Tracespan VDSL Xpert Non-Intrusive Signal Analyzer. This screenshot from the TraceSpan VDSL Xpert shows the R-MSG2 Message that was transmitted by the PACE 5168NV to the CO transceiver. According to the standard in this message the CPE informs the CO whether it supports the optional feature of Interleaver Reconfiguration. The screenshot shows that the PACE 5168NV supports SRA with Interleaver Reconfiguration in the Upstream and Downstream direction.</p>

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<div>U.S. Patent No. 8,462,835</div>	<div>Infringement Allegations</div>
	<div></div>
<div>a transceiver, including a processor, configurable to: transmit a signal using a</div>	<div><div>ITU-T G.993.2 VDSL2 Standard</div><div>The Accused Products comprises a transceiver operable to transmit using a first FIP setting,. See, e.g., ITU-T G.993.2 (12/2011) at Table 12-57:</div></div>

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first FIP setting,	<p>9.1 PMS-TC functional model</p> <p>The PMS-TC functional models are presented in Figure 9-1 applicable to single latency mode and dual latency mode, and Figure 9-2 applicable to single latency with ROC mode. Up to two bearer channels of transmit user data originated by various TPS-TCs, management data originated by the MPS-TC, and NTR data are incoming via the α/β interface in a uniform format, as specified in clause 8.1.2. The incoming user data and the overhead data are multiplexed into one or two latency paths. Each bearer channel is carried over a single latency path (i.e., shall not be split across two latency paths). A Synchbyte is added to each latency path for OH frame alignment.</p> <p>Three different modes are allowed:</p> <ul style="list-style-type: none"> – Single latency mode: support of one latency path. The VTU shall support this mode. For this mode, latency path #0 shall be enabled. – Dual latency mode: support of two latency paths. The VTU may support this mode. For this mode, latency paths #0 and #1 shall be enabled. – Single latency with ROC mode: support of a single latency path for data with a second overhead-only latency path. The VTU may support this mode. For this mode, the data shall use latency path#1 and the ROC shall use latency path #0. <p>NOTE 1 – When transporting two or more applications with different latency and impulse noise protection (INP) requirements and limited higher layer error resilience, a VTU should implement dual latency because, in general, under these conditions dual latency will provide improved performance and/or quality of service.</p> <p>The multiplexed data in each latency path (including the overhead-only latency path, if present) is scrambled, encoded using Reed-Solomon forward error correction coding, and interleaved. The interleaved buffers of data of both latency paths are multiplexed into a bit stream to be submitted to the PMD sublayer via the δ interface.</p>

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	<p>9.3 Forward error correction</p> <p>A standard byte-oriented Reed-Solomon code shall be used for forward error correction (FEC). FEC provides protection against random and burst errors. A Reed-Solomon code word shall contain $N_{FEC} = K + R$ bytes, comprised of R check bytes $c_0, c_1, \dots, c_{R-2}, c_{R-1}$ appended to the K data bytes $m_0, m_1, \dots, m_{K-2}, m_{K-1}$. The check bytes shall be computed from the data bytes using the equation:</p> $C(D) = M(D)D^R \bmod G(D)$ <p>where:</p> <p>$M(D) = m_0D^{K-1} \oplus m_1D^{K-2} \oplus \dots \oplus m_{K-2}D \oplus m_{K-1}$ is the data polynomial</p> <p>$C(D) = c_0D^{R-1} \oplus c_1D^{R-2} \oplus \dots \oplus c_{R-2}D \oplus c_{R-1}$ is the check polynomial</p> <p>$G(D) = \prod (D \oplus \alpha^i)$ is the generator polynomial of the Reed-Solomon code, where the index of the product runs from $i = 0$ to $R-1$</p> <p>The polynomial $C(D)$ is the remainder obtained from dividing $M(D)D^R$ by $G(D)$. The arithmetic shall be performed in the Galois Field GF(256), where α is a primitive element that satisfies the primitive binary polynomial $x^8 \oplus x^4 \oplus x^3 \oplus x^2 \oplus 1$. A data byte $(d_7, d_6, \dots, d_1, d_0)$ is identified with the Galois Field element $d_7\alpha^7 \oplus d_6\alpha^6 \oplus \dots \oplus d_1\alpha \oplus d_0$.</p> <p>Both K and R shall be programmable parameters. Valid values for the number of check bytes R in the codeword are 0, 2, 4, 6, 8, ..., 16. Valid values for the number of bytes in the codeword N_{FEC} (codeword size) are all integers from 32 to 255, inclusive. A VTU shall support all valid values of R and N_{FEC}.</p> <p>The FEC for the ROC shall only use $R=16$ and N_{FEC} values from 32 to 66 with $q = 1$.</p>

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	<p>9.4 Interleaving</p> <p>Interleaving shall be provided in all supported latency paths to protect the data against bursts of errors by spreading the errors over a number of Reed-Solomon codewords. The convolutional interleaver adopted for VDSL2 shall follow the rule:</p> <ul style="list-style-type: none"> – I is the interleaver block size in bytes. Each of the I bytes in an interleaver block $B_0B_1 \dots B_{I-1}$ shall be delayed by the interleaver by an amount that varies linearly with the byte index. More precisely byte B_j (with index j) shall be delayed by $\Delta[j] = (D - 1) \times j$ bytes, where D is the interleaver depth in bytes, and D and I are co-prime (have no common divisor except for 1). <p>For any interleaver input of size $D \times I$ bytes, the relationship between the index of each input byte (n_{in}) and the index of each output byte (n_{out}) is given by $n_{out} = (n_{in} + \Delta[j])$, where $j = n_{in} \bmod I$ and $\Delta[j] = (D - 1) \times j$.</p> <p>The total delay of the interleaver/de-interleaver combination is $(D - 1) \times (I - 1)$ bytes.</p> <p>The RS codeword length N_{FEC} shall be an integer multiple of I, i.e., $N_{FEC} = q \times I$, where q is an integer between 1 and 8 inclusive. All values of q shall be supported. Codewords shall be mapped to interleaver blocks such that the first I bytes of the codeword map to the I bytes $B_0B_1 \dots B_{I-1}$ of the first interleaver block.</p> <p>The interleaver depth shall be set to meet the requirements for error-burst protection and latency. The VTU shall support all integer values of D from 1 to D_{max}, as specified for the particular profile (see Table 6-1). At any data rate, the minimum latency occurs when the interleaver is turned off. If</p>

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<u>U.S. Patent No. 8,462,835</u>	<u>Infringement Allegations</u>																	
	Table 9-3 – Summary of interleaver parameters																	
	<table><tr><th>Parameter(s)</th><th>Value for:<ul style="list-style-type: none">• single latency mode (latency path #0)• dual latency mode (latency paths #0 and #1)• single latency with ROC mode (latency path #1)</th><th>Value for: single latency with ROC mode (latency path #0)</th></tr><tr><td><i>D</i> and <i>I</i></td><td>Co-prime</td><td>Co-prime</td></tr><tr><td><i>q</i></td><td>Integer between 1 and 8, inclusive</td><td>1</td></tr><tr><td><i>N</i>_{FEC}</td><td>Integer between 32 and 255 inclusive, <i>N</i>_{FEC} = <i>q</i> × <i>I</i></td><td>Integer between 32 and 66 inclusive, <i>N</i>_{FEC} = <i>q</i> × <i>I</i></td></tr><tr><td>Total delay of the interleaver/de-interleaver combination</td><td>(<i>D</i>−1) × (<i>I</i>−1) bytes</td><td>(<i>D</i>−1) × (<i>I</i>−1) bytes</td></tr></table>	Parameter(s)	Value for: <ul style="list-style-type: none">• single latency mode (latency path #0)• dual latency mode (latency paths #0 and #1)• single latency with ROC mode (latency path #1)	Value for: single latency with ROC mode (latency path #0)	<i>D</i> and <i>I</i>	Co-prime	Co-prime	<i>q</i>	Integer between 1 and 8, inclusive	1	<i>N</i> _{FEC}	Integer between 32 and 255 inclusive, <i>N</i> _{FEC} = <i>q</i> × <i>I</i>	Integer between 32 and 66 inclusive, <i>N</i> _{FEC} = <i>q</i> × <i>I</i>	Total delay of the interleaver/de-interleaver combination	(<i>D</i> −1) × (<i>I</i> −1) bytes	(<i>D</i> −1) × (<i>I</i> −1) bytes		
Parameter(s)	Value for: <ul style="list-style-type: none">• single latency mode (latency path #0)• dual latency mode (latency paths #0 and #1)• single latency with ROC mode (latency path #1)	Value for: single latency with ROC mode (latency path #0)																
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<i>q</i>	Integer between 1 and 8, inclusive	1																
<i>N</i> _{FEC}	Integer between 32 and 255 inclusive, <i>N</i> _{FEC} = <i>q</i> × <i>I</i>	Integer between 32 and 66 inclusive, <i>N</i> _{FEC} = <i>q</i> × <i>I</i>																
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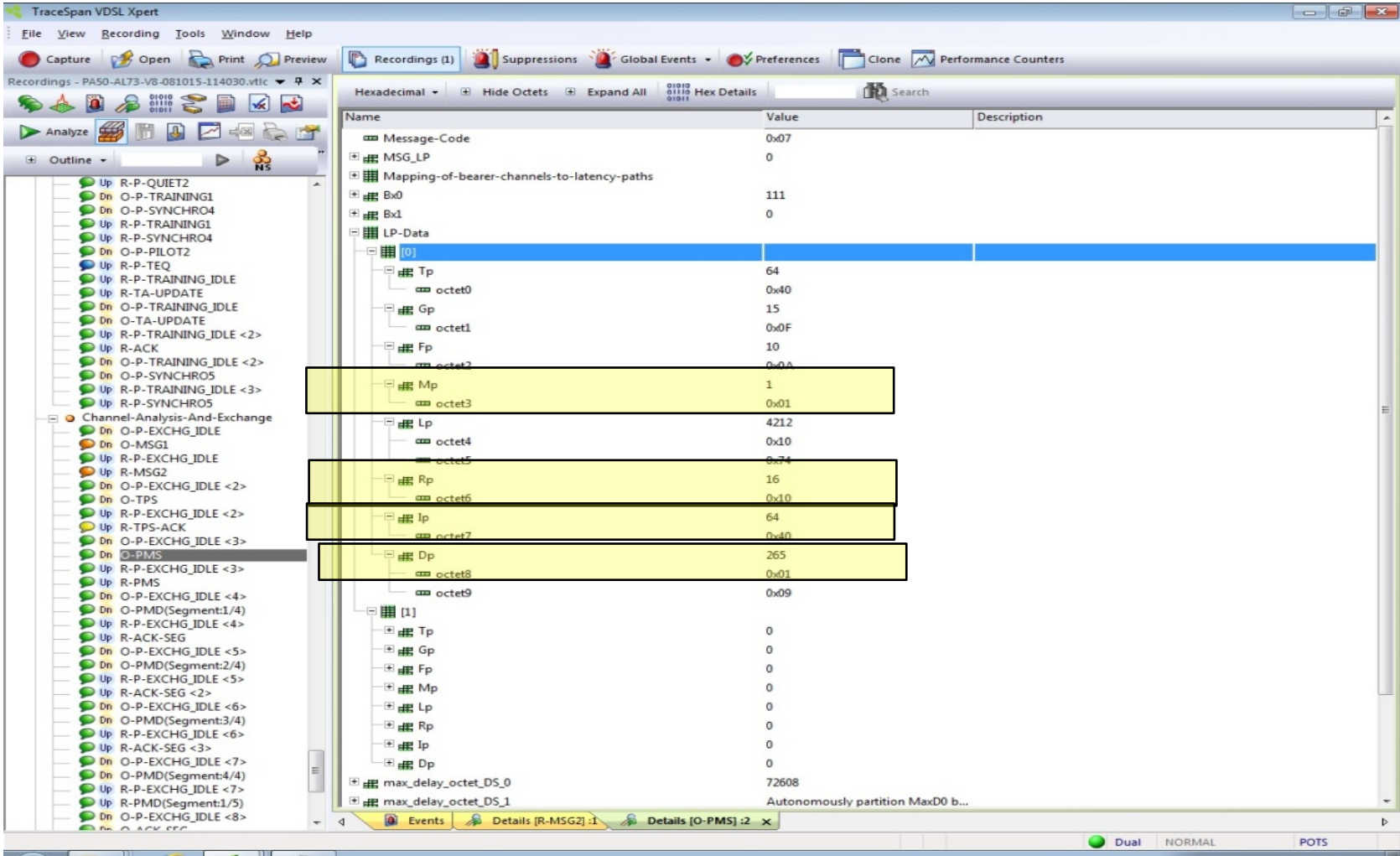
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	<div>12.3.5.2.1.3 O-PMS</div> <div>The O-PMS message conveys the initial PMS-TC parameter settings that shall be used in the upstream direction during Showtime. It also specifies the portion of shared interleaver memory that the VTU-R can use to de-interleave the downstream data stream. The full list of parameters carried by the O-PMS message is shown in Table 12-56.</div> <div>Table 12-56 – Description of message O-PMS</div> <table><tr><th></th><th>Field name</th><th>Format</th></tr><tr><td>1</td><td>Message descriptor</td><td>Message code</td></tr><tr><td>2</td><td>MSGLP (Note 1)</td><td>1 byte</td></tr><tr><td>3</td><td>Mapping of bearer channels to latency paths</td><td>1 byte</td></tr><tr><td>4</td><td>B_{x0}</td><td>1 byte</td></tr><tr><td>5</td><td>B_{x1}</td><td>1 byte</td></tr><tr><td>6</td><td>LP₀ (Note 2)</td><td>Latency path descriptor</td></tr><tr><td>7</td><td>LP₁</td><td>Latency path descriptor</td></tr><tr><td>8</td><td>max_delay_octet_{DS,0}</td><td>3 bytes</td></tr><tr><td>9</td><td>max_delay_octet_{DS,1}</td><td>3 bytes</td></tr><tr><td>10</td><td>max_delay_octet_{US,0}</td><td>3 bytes</td></tr><tr><td>11</td><td>max_delay_octet_{US,1}</td><td>3 bytes</td></tr><tr><td>12</td><td>Upstream SOS tone groups</td><td>Band descriptor</td></tr><tr><td>13</td><td>Upstream ROC parameters</td><td>ROC descriptor</td></tr><tr><td>14</td><td>ITU-T G.998.4 parameter field</td><td>Variable length</td></tr><tr><td>15</td><td>ITU-T G.993.5 parameter field</td><td>Variable length</td></tr><tr><td>16</td><td>ATTNDR_max_delay_octets_{DS,p}</td><td>3 bytes</td></tr></table> <div>NOTE 1 – If the ROC is enabled, MSGLP shall be equal to 0. NOTE 2 – If the ROC is enabled, the framing parameters for latency path #0 shall be contained in the ROC descriptor.</div>		Field name	Format	1	Message descriptor	Message code	2	MSGLP (Note 1)	1 byte	3	Mapping of bearer channels to latency paths	1 byte	4	B _{x0}	1 byte	5	B _{x1}	1 byte	6	LP ₀ (Note 2)	Latency path descriptor	7	LP ₁	Latency path descriptor	8	max_delay_octet _{DS,0}	3 bytes	9	max_delay_octet _{DS,1}	3 bytes	10	max_delay_octet _{US,0}	3 bytes	11	max_delay_octet _{US,1}	3 bytes	12	Upstream SOS tone groups	Band descriptor	13	Upstream ROC parameters	ROC descriptor	14	ITU-T G.998.4 parameter field	Variable length	15	ITU-T G.993.5 parameter field	Variable length	16	ATTNDR_max_delay_octets _{DS,p}	3 bytes
	Field name	Format																																																		
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	<p>Field #6 "LP₀" is a 10-byte field that contains the PMS-TC parameters for latency path #0 in the upstream direction. The "Latency path descriptor" format specified in Table 12-57 shall be used.</p> <p>Field #7 "LP₁" is a 10-byte field that contains the PMS-TC parameters for latency path #1 in the upstream direction. The "Latency path descriptor" format specified in Table 12-57 shall be used. If latency path #1 is not used, all bytes of LP₁ shall be set to ZERO.</p> <p style="text-align: center;">Table 12-57 – Latency path descriptor</p> <table><tr><th>Octet</th><th>Field</th><th>Format</th><th>Description</th></tr><tr><td>4</td><td>M</td><td>1 byte</td><td>The number of MDFs in an RS codeword for the latency path. Only the values 1, 2, 4, 8, 16 are allowable.</td></tr><tr><td>5 and 6</td><td>L</td><td>2 bytes</td><td>Contains the value of <i>L</i> for the latency path.</td></tr><tr><td>7</td><td>R</td><td>1 byte</td><td>Contains the value of <i>R</i> for the latency path.</td></tr><tr><td>8</td><td>I</td><td>1 byte</td><td>Contains the value of <i>I</i> for the latency path.</td></tr><tr><td>9 and 10</td><td>D</td><td>2 bytes</td><td>Interleaver depth <i>D</i> for the latency path.</td></tr></table> <p>Also see, e.g., ITU-T G.993.2 (02/2019) at Table 12-57:</p> <p><u>Testing</u></p> <p>This screenshot from the TraceSpan VDSL Xpert shows the O-PMS Message received by the PACE 5168NV from the CO transceiver. In this message the CO transceiver sends to the PACE 5168NV the FIP settings (FEC and Interleaver parameter values) that the PACE 5168NV will use to transmit upstream signals. The screenshot shows that the first FIP setting is [Mp=1,</p>	Octet	Field	Format	Description	4	M	1 byte	The number of MDFs in an RS codeword for the latency path. Only the values 1, 2, 4, 8, 16 are allowable.	5 and 6	L	2 bytes	Contains the value of <i>L</i> for the latency path.	7	R	1 byte	Contains the value of <i>R</i> for the latency path.	8	I	1 byte	Contains the value of <i>I</i> for the latency path.	9 and 10	D	2 bytes	Interleaver depth <i>D</i> for the latency path.
Octet	Field	Format	Description																						
4	M	1 byte	The number of MDFs in an RS codeword for the latency path. Only the values 1, 2, 4, 8, 16 are allowable.																						
5 and 6	L	2 bytes	Contains the value of <i>L</i> for the latency path.																						
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	<p>Rp=16, Ip=64, Dp=265].</p> 
transmit a flag signal, and	<u>ITU-T G.993.2 VDSL2 Standard</u>

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	<p>The Accused Products comprises a transceiver operable to transmit a flag signal. See, e.g., ITU-T G.993.2 (12/2011) at § 3.64 Syncflag, § 10.5.3 On-line reconfiguration:</p> <p>3.64 Syncflag: A sync symbol in which the sync frame bits are inverted relative to the sync frame modulated by the most recently transmitted sync symbol (i.e., if the previous sync frame was all ZEROS, the Syncflag would correspond to a sync frame of all ONES, and vice versa). The Syncflag is used to signal online reconfiguration transitions.</p> <p>10.5.3 On-line reconfiguration</p> <p>The transmitter inserts a sync symbol every 257 symbols, as defined in clause 10.2. Therefore, a sync symbol shall be transmitted after every 256 data symbols.</p> <p>To signal on-line reconfiguration timing (see clause 13.3), the responding VTU shall send a Syncflag (see clause 3.64).</p> <p>See, e.g., ITU-T G.993.2 (02/2019) at § 3.64 Syncflag, § 10.5.3 On-line reconfiguration</p> <p><u>Testing</u></p> <p>This screenshot from the TraceSpan VDSL Xpert shows the Sync Flag signal transmitted by the PACE 5168NV in response to the On Line Reconfiguration Request Type 3 message from CO transceiver. The On Line Reconfiguration Request Type 3 message is a Seamless Rate Adaptation (SRA) Message that includes the new FIP setting.</p>

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switch to using
for
transmission, a
second FIP
setting
following

ITU-T G.993.2 VDSL2 Standard

The Accused Products comprises a transceiver operable to switch to using for transmission, a second FIP setting. See, e.g., ITU-T G.993.2 (12/2011) at § 13.3 Timing of changes in subcarrier configuration:

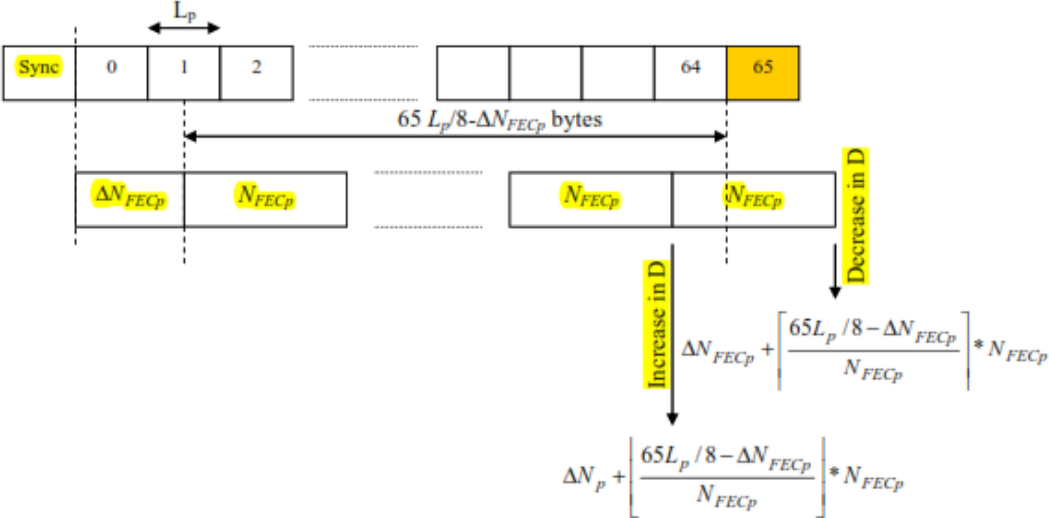
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transmission of the flag signal,	Table 11-6 – OLR commands sent by the initiating VTU				
	Name	Length (octets)	Octet number	Content	Support
	Request Type 1	$5 + 4 \times N_f$ ($N_f \leq 128$)	2	04 ₁₆ (Note 1)	Mandatory
			3 to 4	2 octets for the number of subcarriers N_f to be modified	
			5 to 4 + 4 × N_f	4 × N_f octets describing the subcarrier parameter field for each subcarrier	
			5 + 4 × N_f	1 octet for SC	
	Request Type 2	For further study	2	05 ₁₆ (Note 1)	For further study
			All others	Reserved by ITU-T	
	Request Type 3 (SRA) (Note 6)	$5 + 7 N_{LP} + 4 N_f$ ($N_f \leq 128$)	2	06 ₁₆ (Note 1)	Optional
			3 to 2 + 2 N_{LP}	2 × N_{LP} octets containing the new L_p values for each of the active latency paths (N_{LP} = number of active latency paths) (Notes 2 and 3)	
			3 + 2 N_{LP} to 2 + 4 N_{LP}	2 × N_{LP} octets containing the new D_p values for each of the active latency paths (N_{LP} = number of active latency paths) (Note 4)	
			3 + 4 N_{LP} to 2 + 5 N_{LP}	N_{LP} octets containing the new T_p values for each of the active latency paths (N_{LP} = number of active latency paths) (Notes 2, 3, 5)	
			3 + 5 N_{LP} to 2 + 6 N_{LP}	N_{LP} octets containing the new G_p values for each of the active latency paths (N_{LP} = number of active latency paths) (Notes 2, 3, 5)	

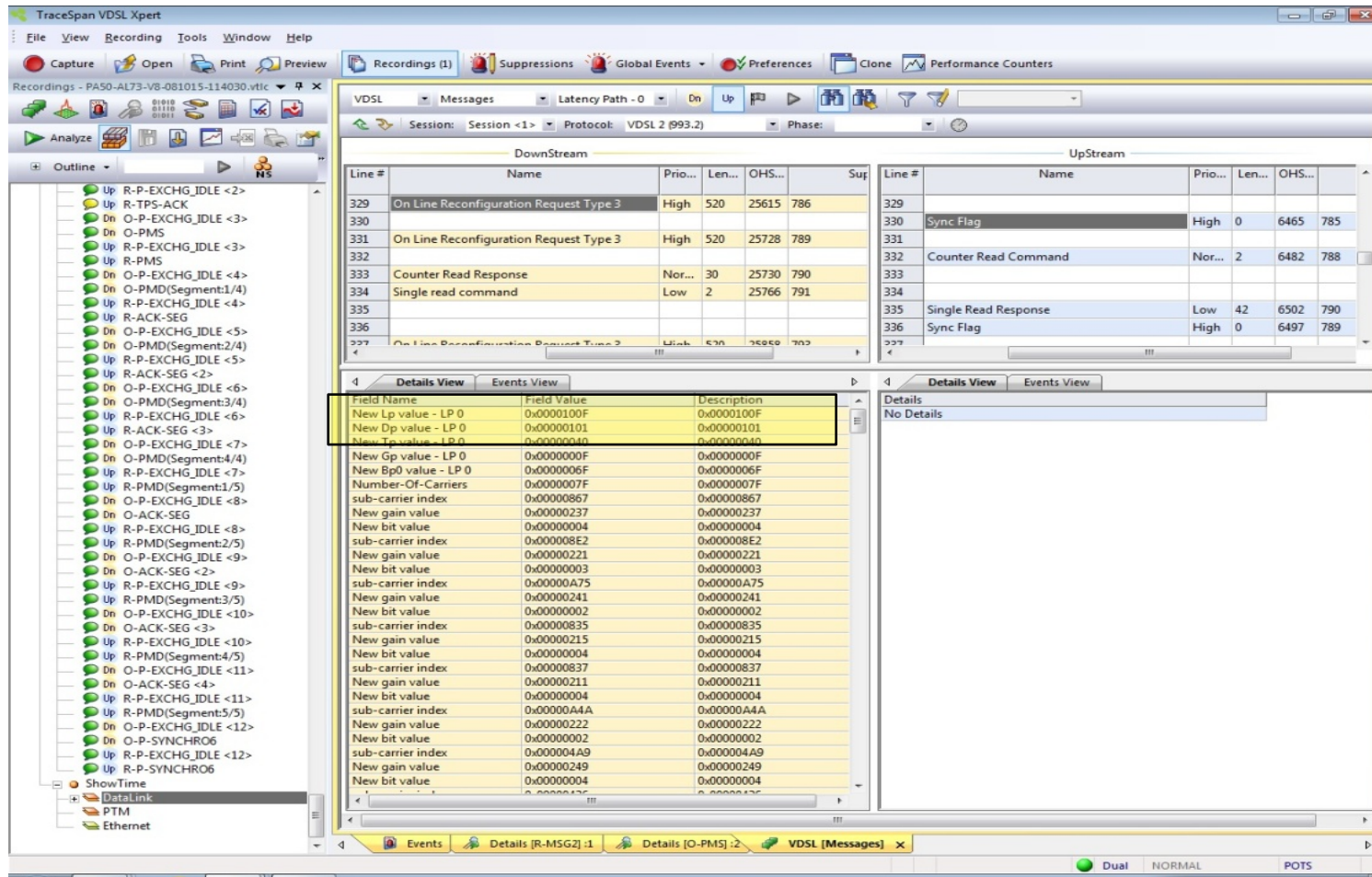
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	<p>13.3 Timing of changes in subcarrier configuration</p> <p>In both the upstream and the downstream directions, the reconfiguration of the PMD functions shall take effect starting with the tenth symbol that follows transport of the Syncflag for OLR type 1. As defined in clause 10.2, the sync symbol is transmitted after every 256 data symbols. The reconfiguration of the PMD function shall take effect starting with the symbol at symbol count 9 in the next DMT superframe, where the first symbol in each DMT superframe is the symbol at symbol count 0.</p>

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	 <p style="text-align: center;">Figure 13-1 – Finding the byte where the change in D_p is activated</p> <p>Figure 13-1 shows the DMT symbol counter and the byte counter at which the interleaver depth change is activated, relative to the Syncflag. For an increase in depth, the change in D_p will always happen at the same time or before the change in L_p, but as close to it as possible (i.e., the change in D_p happens during the DMT symbol with count 64 or sooner). Likewise, for a decrease in depth, the change in D_p will always happen at the same time or after the change in L_p, but as close to it as possible (i.e., the change in D_p happens during the DMT symbol with count 65 or later).</p> <p>Also see, e.g., ITU-T G.993.2 (02/2019) at § 13.3 Timing of changes in subcarrier configuration:</p> <p>Testing</p> <p>This screenshot from the TraceSpan VDSL Xpert shows the On Line Reconfiguration Request Type 3 message received by the PACE 5168NV from CO transceiver that includes the new FIP setting. This new FIP setting will be used by the PACE 5168NV after the transmission of the flag signal. The new FIP setting has a new value for D_p (the interleaver depth). Recall from above that the interleaver depth sent in the O-PMS message was 265 (decimal format). The new interleaver depth in the message below is 101 (HEX format) which is equal to 257 (decimal format). This means that the first FIP setting of [$M_p=1$, $R_p=16$, $I_p=64$, $D_p=265$] was changed to a second FIP setting of [$M_p=1$, $R_p=16$, $I_p=64$, $D_p=257$].</p>

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the first FIP setting comprises at least one first FIP value,

ITU-T G.993.2 VDSL2 Standard

In the Accused Product the first FIP setting comprises at least one first FIP value, the second FIP setting comprises at least one second FIP value, different than the first FIP value See, e.g., ITU-T G.993.2 (12/2011) at § 9.4.1 Dynamic change of interleaver depth:

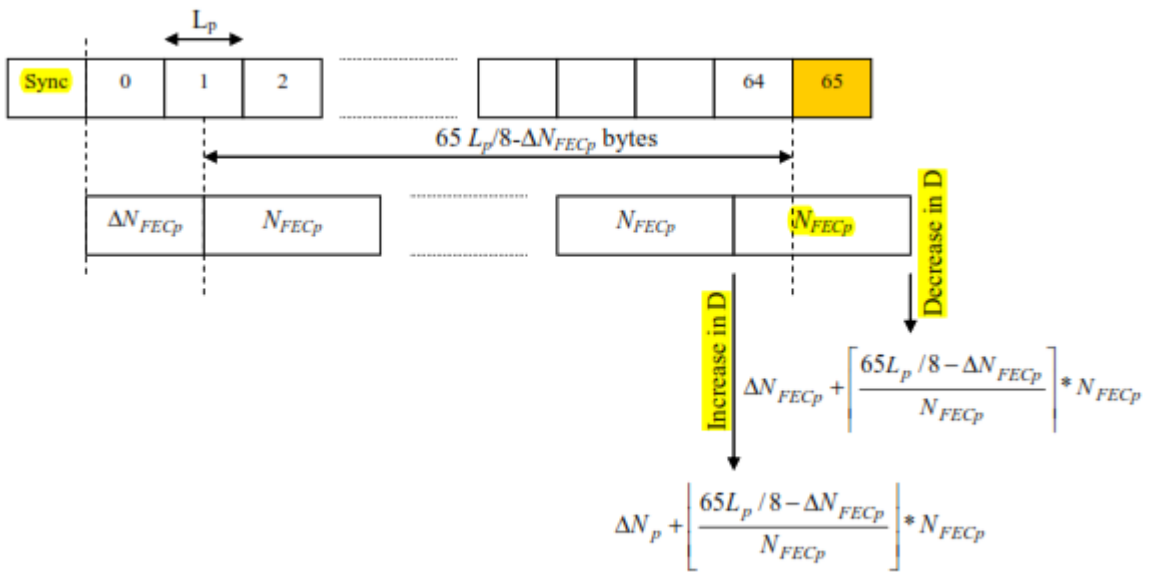
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the second FIP setting comprises at least one second FIP value, different than the first FIP value, and	<p>9.4.1 Dynamic change of interleaver depth</p> <p>A method to dynamically change the interleaver depth during transmission is defined for VDSL2. This method is optional. Support shall be indicated during initialization in O-MSG 1 and R-MSG 2.</p> <p>NOTE – Although this clause defines the procedure for dynamically changing the interleaver depth during transmission, the control command for initiating this procedure is not defined in this version of in this Recommendation. The calling procedure for dynamic change of interleaver depth will be defined in a future revision to this Recommendation.</p> <p>A change of the interleaver depth shall only be initiated at the first byte of an RS codeword, where k is the sequence number of this byte at the input of the interleaver.</p> <p>For an increase of the interleaver depth from D_{old} to D_{new} with $D_{old} < D_{new}$ the interleaver output is defined by:</p> $y(n + \Delta_{old}[j]) = x(n); \text{ for } n + \Delta_{old}(j) < k, \text{ where } \Delta_{old}[j] = (D_{old} - 1) \times j$ $y(n + \Delta_{new}[j]) = x(n); \text{ for } n + \Delta_{old}(j) \geq k, \text{ where } \Delta_{new}[j] = (D_{new} - 1) \times j$ <p>For a decrease of the interleaver depth from D_{old} to D_{new} with $D_{old} > D_{new}$ the interleaver output is defined by:</p> $y(n + \Delta_{old}[j]) = x(n); \text{ for } n + \Delta_{new}(j) + \delta < k$ $y(n + \Delta_{new}[j] + \delta) = x(n); \text{ for } n + \Delta_{new}(j) + \delta \geq k$ <p>where δ is the length of the transition and is given by:</p> $\delta = \lceil (D_{old} - D_{new}) \cdot (I - 1) / I \rceil \cdot I$ <p>Also see, e.g., ITU-T G.993.2 (02/2019) at § 9.4.1 Dynamic change of interleaver depth:</p> <p><u>Testing</u></p> <p>The Tracespan screenshots showed a first FIP setting is [Mp=1, Rp=16, Ip=64, Dp=265] and a second FIP setting is [Mp=1, Rp=16, Ip=64, Dp=257]. The “at least one first FIP value” is Dp=265 and the “at least one second FIP value, different than the first FIP value” is the Dp=257.</p>

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the switching occurs on a pre-defined forward error correction codeword boundary following the flag signal.	<p><u>ITU-T G.993.2 VDSL2 Standard</u></p> <p>In the Accused Products the switching occurs on a pre-defined forward error correction codeword boundary following the flag signal. See, e.g., ITU-T G.993.2 (12/2011) at § 13.3 Timing of changes in subcarrier configuration, Fig. 13-1:</p> <p>13.3 Timing of changes in subcarrier configuration</p> <p>In both the upstream and the downstream directions, the reconfiguration of the PMD functions shall take effect starting with the tenth symbol that follows transport of the Syncflag for OLR type 1. As defined in clause 10.2, the sync symbol is transmitted after every 256 data symbols. The reconfiguration of the PMD function shall take effect starting with the symbol at symbol count 9 in the next DMT superframe, where the first symbol in each DMT superframe is the symbol at symbol count 0.</p> <p>For OLR Type 3, when performed in the latency path p, the change in L_p values and b_i, g_i values shall take effect starting from the 66th symbol that follows the Syncflag, i.e., the symbol with symbol count 65 in the DMT superframe following the Syncflag, where the first symbol in the DMT superframe is the symbol at symbol count 0.</p> <p>The change of framing parameters T_p, G_p and B_{p0} shall take effect on the first OH frame of the first OH superframe that follows the 66th DMT symbol after the Syncflag.</p> <p>The change in D_p shall take effect on the first byte of an interleaved RS codeword (byte k as defined in clause 9.4.1). This codeword shall be determined as follows:</p> <ul style="list-style-type: none"> • For a decrease in interleaver depth, this shall be the first RS codeword that starts at or after the beginning of the 66th DMT symbol. • For an increase in interleaver depth, this shall be the last RS codeword that starts at or before the beginning of the 66th DMT symbol.

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	 <p style="text-align: center;">Figure 13-1 – Finding the byte where the change in D_p is activated</p> <p>See, e.g., ITU-T G.993.2 (02/2019) at § 13.3 Timing of changes in subcarrier configuration, Fig. 13-1:</p>
10. The apparatus of claim 8, wherein a first interleaver parameter value of the first FIP setting is	<p><u>ITU-T G.993.2 VDSL2 Standard</u></p> <p>The Accused Products comprise an apparatus, wherein a first interleaver parameter value of the first FIP setting is different than a second interleaver parameter value of the second FIP setting. See, e.g., ITU-T G.993.2 (12/2011) at § 9.4.1, Dynamic change of interleaver depth:</p>

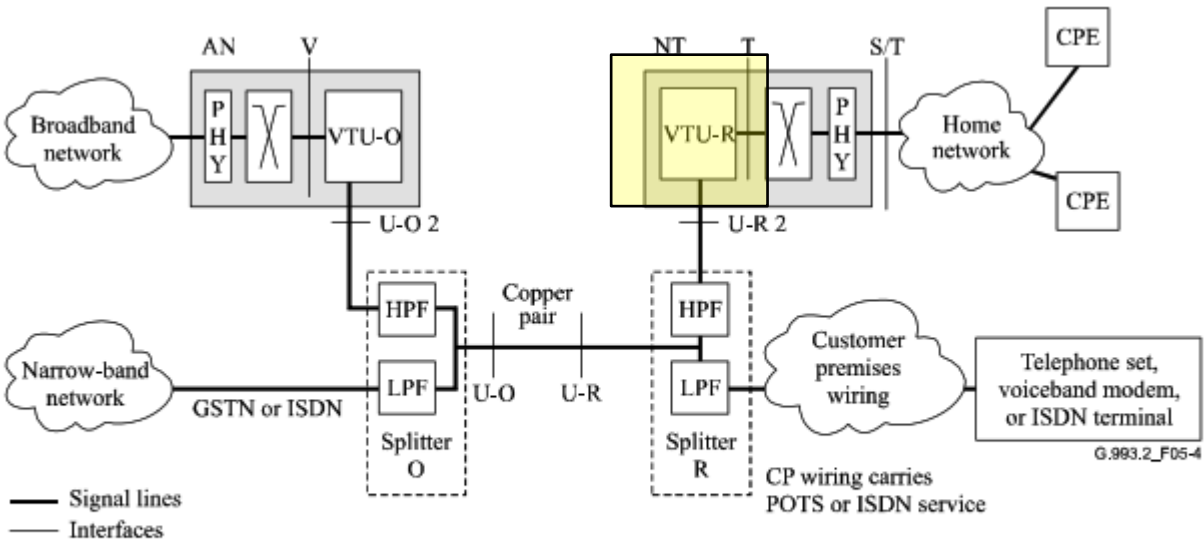
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different than a second interleaver parameter value of the second FIP setting.	<p>9.4.1 Dynamic change of interleaver depth</p> <p>A method to dynamically change the interleaver depth during transmission is defined for VDSL2. This method is optional. Support shall be indicated during initialization in O-MSG 1 and R-MSG 2.</p> <p>NOTE – Although this clause defines the procedure for dynamically changing the interleaver depth during transmission, the control command for initiating this procedure is not defined in this version of in this Recommendation. The calling procedure for dynamic change of interleaver depth will be defined in a future revision to this Recommendation.</p> <p>A change of the interleaver depth shall only be initiated at the first byte of an RS codeword, where k is the sequence number of this byte at the input of the interleaver.</p> <p>For an increase of the interleaver depth from D_{old} to D_{new} with $D_{old} < D_{new}$ the interleaver output is defined by:</p> $y(n + \Delta_{old}[j]) = x(n); \text{ for } n + \Delta_{old}(j) < k, \text{ where } \Delta_{old}[j] = (D_{old} - 1) \times j$ $y(n + \Delta_{new}[j]) = x(n); \text{ for } n + \Delta_{old}(j) \geq k, \text{ where } \Delta_{new}[j] = (D_{new} - 1) \times j$ <p>For a decrease of the interleaver depth from D_{old} to D_{new} with $D_{old} > D_{new}$ the interleaver output is defined by:</p> $y(n + \Delta_{old}[j]) = x(n); \text{ for } n + \Delta_{new}(j) + \delta < k$ $y(n + \Delta_{new}[j] + \delta) = x(n); \text{ for } n + \Delta_{new}(j) + \delta \geq k$ <p>where δ is the length of the transition and is given by:</p> $\delta = \lceil (D_{old} - D_{new}) \cdot (I - 1) / I \rceil \cdot I$ <p>See also, e.g., ITU-T G.993.2 (02/2019) at § 9.4.1, Dynamic change of interleaver depth:</p> <p><u>Testing</u></p> <p>The Tracespan screenshots showed that interleaver depth was changed from 265 to 257.</p>
24. An apparatus configurable to	<u>ITU-T G.993.2 VDSL2 Standard</u>

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adapt forward error correction and interleaver parameter (FIP) settings during steady-state communication or initialization comprising:	<p>The Accused Products operate in accordance with the VDSL2 (i.e., ITU-T G.993.2) standard comprise an apparatus configurable to adapt forward error correction and interleaver parameter (FIP) settings during steady-state communication or initialization. See, e.g., ITU-T G.993.2 (12/2011) at § 9.4.1 <i>Dynamic change of interleaver depth</i>:</p> <div data-bbox="373 500 730 690"> <p>ITU-T</p> <p>TELECOMMUNICATION STANDARDIZATION SECTOR OF ITU</p> </div> <div data-bbox="1161 509 1432 630"> <p>G.993.2</p> <p>(12/2011)</p> </div> <p>SERIES G: TRANSMISSION SYSTEMS AND MEDIA, DIGITAL SYSTEMS AND NETWORKS</p> <p>Digital sections and digital line system – Access networks</p> <hr/> <p>Very high speed digital subscriber line transceivers 2 (VDSL2)</p>

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	 <p>Figure 5-4 – Generic application reference model for remote deployment with splitter</p>

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	<p>Recommendation ITU-T G.993.2</p> <p>Very high speed digital subscriber line transceivers 2 (VDSL2)</p> <p>1 Scope</p> <p>This Recommendation is an enhancement to [ITU-T G.993.1] that supports transmission at a bidirectional net data rate (the sum of upstream and downstream rates) up to 200 Mbit/s on twisted pairs. This Recommendation is an access technology that exploits the existing infrastructure of copper wires that were originally deployed for POTS (plain old telephone service).</p> <p>This Recommendation specifies only discrete multi-tone (DMT) modulation and incorporates components from [ITU-T G.993.1] (VDSL), [ITU-T G.992.3] (ADSL2), and [ITU-T G.992.5] (ADSL2 plus).</p> <p>...</p> <p>For PMS-TC sublayer specifically, changes in this Recommendation relative to [ITU-T G.993.1] include:</p> <ul style="list-style-type: none"> • Improved framing (based on [ITU-T G.992.3]); • The definition of two latency paths and two bearer channels; • Improved OLR mechanisms (based on [ITU-T G.992.3]), including optional SRA, SOS, and dynamic interleaver change; <p>9.4.1 Dynamic change of interleaver depth</p> <p>A method to dynamically change the interleaver depth during transmission is defined for VDSL2. This method is optional. Support shall be indicated during initialization in O-MSG 1 and R-MSG 2.</p> <p><i>See also, e.g., ITU-T G.993.2 (02/2019 at § 9.4.1 Dynamic change of interleaver depth:</i></p> <p><u>Product Documentation</u></p>

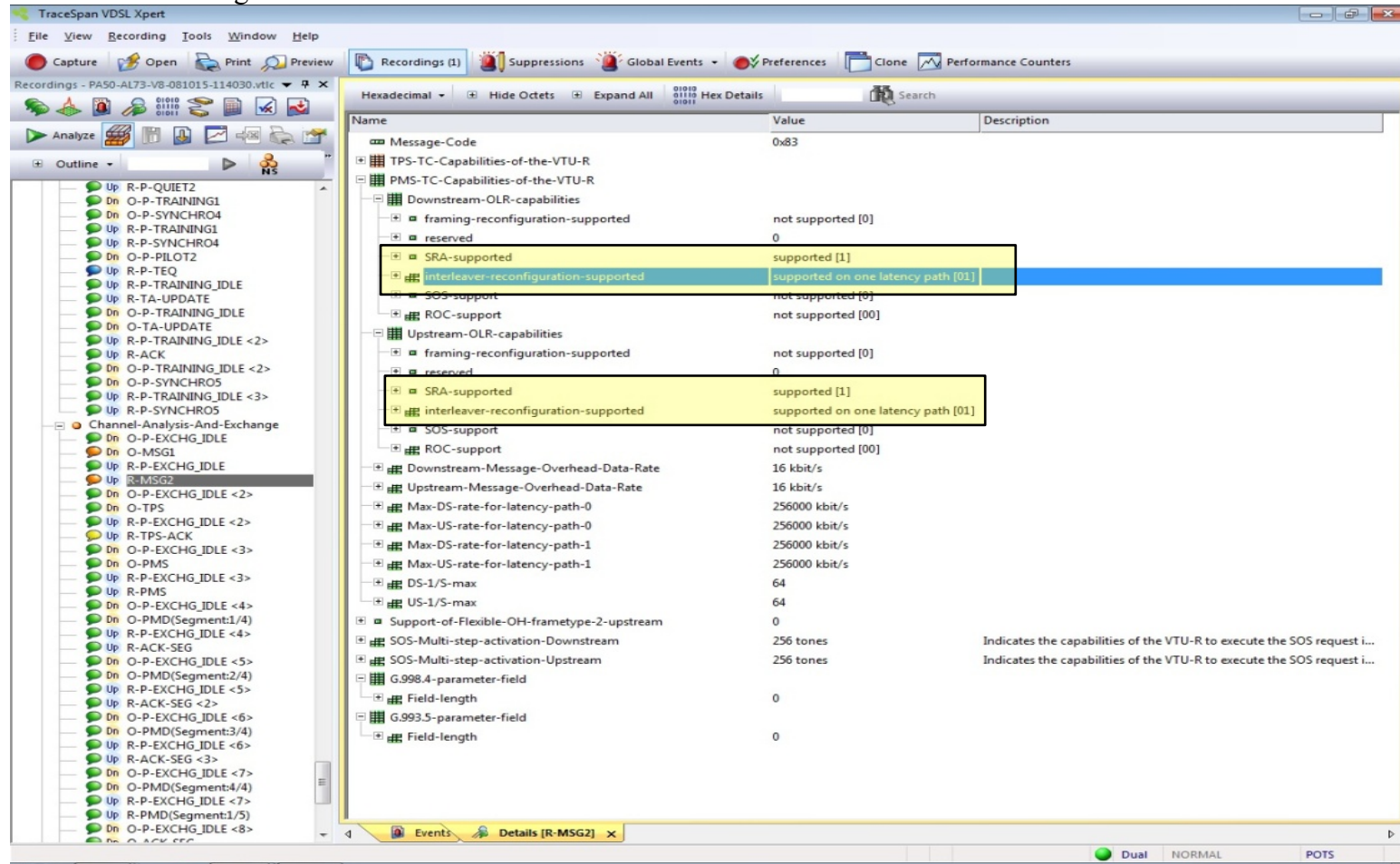
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Testing

Testing of the upstream direction showed that the Pace 5168NV supports SRA with interleaver reconfiguration in the downstream direction. The screenshot from the Tracespan VDSL Xpert shows that the PACE 5168NV supports SRA with Interleaver Reconfiguration in the Downstream direction.



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<p>a transceiver, including a processor, configurable to:</p> <p>receive a signal using a first FIP setting,</p>	<p><u>ITU-T G.993.2 VDSL2 Standard</u></p> <p>The Accused Products comprises a transceiver configurable to receive using a first FIP setting,. See, e.g., ITU-T G.993.2 (12/2011) at Table 12-57:</p> <p>9.1 PMS-TC functional model</p> <p>The PMS-TC functional models are presented in Figure 9-1 applicable to single latency mode and dual latency mode, and Figure 9-2 applicable to single latency with ROC mode. Up to two bearer channels of transmit user data originated by various TPS-TCs, management data originated by the MPS-TC, and NTR data are incoming via the α/β interface in a uniform format, as specified in clause 8.1.2. The incoming user data and the overhead data are multiplexed into one or two latency paths. Each bearer channel is carried over a single latency path (i.e., shall not be split across two latency paths). A Syncbyte is added to each latency path for OH frame alignment.</p> <p>Three different modes are allowed:</p> <ul style="list-style-type: none"> – Single latency mode: support of one latency path. The VTU shall support this mode. For this mode, latency path #0 shall be enabled. – Dual latency mode: support of two latency paths. The VTU may support this mode. For this mode, latency paths #0 and #1 shall be enabled. – Single latency with ROC mode: support of a single latency path for data with a second overhead-only latency path. The VTU may support this mode. For this mode, the data shall use latency path#1 and the ROC shall use latency path #0. <p>NOTE 1 – When transporting two or more applications with different latency and impulse noise protection (INP) requirements and limited higher layer error resilience, a VTU should implement dual latency because, in general, under these conditions dual latency will provide improved performance and/or quality of service.</p> <p>The multiplexed data in each latency path (including the overhead-only latency path, if present) is scrambled, encoded using Reed-Solomon forward error correction coding, and interleaved. The interleaved buffers of data of both latency paths are multiplexed into a bit stream to be submitted to the PMD sublayer via the δ interface.</p>

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	<p>9.3 Forward error correction</p> <p>A standard byte-oriented Reed-Solomon code shall be used for forward error correction (FEC). FEC provides protection against random and burst errors. A Reed-Solomon code word shall contain $N_{FEC} = K + R$ bytes, comprised of R check bytes $c_0, c_1, \dots, c_{R-2}, c_{R-1}$ appended to the K data bytes $m_0, m_1, \dots, m_{K-2}, m_{K-1}$. The check bytes shall be computed from the data bytes using the equation:</p> $C(D) = M(D)D^R \bmod G(D)$ <p>where:</p> <p>$M(D) = m_0D^{K-1} \oplus m_1D^{K-2} \oplus \dots \oplus m_{K-2}D \oplus m_{K-1}$ is the data polynomial</p> <p>$C(D) = c_0D^{R-1} \oplus c_1D^{R-2} \oplus \dots \oplus c_{R-2}D \oplus c_{R-1}$ is the check polynomial</p> <p>$G(D) = \prod (D \oplus \alpha^i)$ is the generator polynomial of the Reed-Solomon code, where the index of the product runs from $i = 0$ to $R-1$</p> <p>The polynomial $C(D)$ is the remainder obtained from dividing $M(D)D^R$ by $G(D)$. The arithmetic shall be performed in the Galois Field GF(256), where α is a primitive element that satisfies the primitive binary polynomial $x^8 \oplus x^4 \oplus x^3 \oplus x^2 \oplus 1$. A data byte $(d_7, d_6, \dots, d_1, d_0)$ is identified with the Galois Field element $d_7\alpha^7 \oplus d_6\alpha^6 \oplus \dots \oplus d_1\alpha \oplus d_0$.</p> <p>Both K and R shall be programmable parameters. Valid values for the number of check bytes R in the codeword are 0, 2, 4, 6, 8, ..., 16. Valid values for the number of bytes in the codeword N_{FEC} (codeword size) are all integers from 32 to 255, inclusive. A VTU shall support all valid values of R and N_{FEC}.</p> <p>The FEC for the ROC shall only use $R=16$ and N_{FEC} values from 32 to 66 with $q = 1$.</p>

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	<p>9.4 Interleaving</p> <p>Interleaving shall be provided in all supported latency paths to protect the data against bursts of errors by spreading the errors over a number of Reed-Solomon codewords. The convolutional interleaver adopted for VDSL2 shall follow the rule:</p> <ul style="list-style-type: none"> – I is the interleaver block size in bytes. Each of the I bytes in an interleaver block $B_0B_1 \dots B_{I-1}$ shall be delayed by the interleaver by an amount that varies linearly with the byte index. More precisely byte B_j (with index j) shall be delayed by $\Delta[j] = (D - 1) \times j$ bytes, where D is the interleaver depth in bytes, and D and I are co-prime (have no common divisor except for 1). <p>For any interleaver input of size $D \times I$ bytes, the relationship between the index of each input byte (n_{in}) and the index of each output byte (n_{out}) is given by $n_{out} = (n_{in} + \Delta[j])$, where $j = n_{in} \bmod I$ and $\Delta[j] = (D - 1) \times j$.</p> <p>The total delay of the interleaver/de-interleaver combination is $(D - 1) \times (I - 1)$ bytes.</p> <p>The RS codeword length N_{FEC} shall be an integer multiple of I, i.e., $N_{FEC} = q \times I$, where q is an integer between 1 and 8 inclusive. All values of q shall be supported. Codewords shall be mapped to interleaver blocks such that the first I bytes of the codeword map to the I bytes $B_0B_1 \dots B_{I-1}$ of the first interleaver block.</p> <p>The interleaver depth shall be set to meet the requirements for error-burst protection and latency. The VTU shall support all integer values of D from 1 to D_{max}, as specified for the particular profile (see Table 6-1). At any data rate, the minimum latency occurs when the interleaver is turned off. If</p>

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	Table 9-3 – Summary of interleaver parameters																	
	<table><tr><th>Parameter(s)</th><th>Value for:<ul style="list-style-type: none">single latency mode (latency path #0)dual latency mode (latency paths #0 and #1)single latency with ROC mode (latency path #1)</th><th>Value for: single latency with ROC mode (latency path #0)</th></tr><tr><td>D and I</td><td>Co-prime</td><td>Co-prime</td></tr><tr><td>q</td><td>Integer between 1 and 8, inclusive</td><td>1</td></tr><tr><td>N_{FEC}</td><td>Integer between 32 and 255 inclusive, N_{FEC} = q × I</td><td>Integer between 32 and 66 inclusive, N_{FEC} = q × I</td></tr><tr><td>Total delay of the interleaver/de-interleaver combination</td><td>(D–1) × (I–1) bytes</td><td>(D–1) × (I–1) bytes</td></tr></table>			Parameter(s)	Value for: <ul style="list-style-type: none">single latency mode (latency path #0)dual latency mode (latency paths #0 and #1)single latency with ROC mode (latency path #1)	Value for: single latency with ROC mode (latency path #0)	D and I	Co-prime	Co-prime	q	Integer between 1 and 8, inclusive	1	N _{FEC}	Integer between 32 and 255 inclusive, N _{FEC} = q × I	Integer between 32 and 66 inclusive, N _{FEC} = q × I	Total delay of the interleaver/de-interleaver combination	(D–1) × (I–1) bytes	(D–1) × (I–1) bytes
Parameter(s)	Value for: <ul style="list-style-type: none">single latency mode (latency path #0)dual latency mode (latency paths #0 and #1)single latency with ROC mode (latency path #1)	Value for: single latency with ROC mode (latency path #0)																
D and I	Co-prime	Co-prime																
q	Integer between 1 and 8, inclusive	1																
N _{FEC}	Integer between 32 and 255 inclusive, N _{FEC} = q × I	Integer between 32 and 66 inclusive, N _{FEC} = q × I																
Total delay of the interleaver/de-interleaver combination	(D–1) × (I–1) bytes	(D–1) × (I–1) bytes																
	<p>12.3.5.2.2.3 R-PMS</p> <p>The R-PMS message conveys the initial PMS-TC parameter settings that shall be used in the downstream direction during showtime. The full list of parameters carried by the R-PMS message is shown in Table 12-64.</p>																	

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	<p>Table 12-64 – Description of message R-PMS</p> <table><tr><td></td><td>Field name</td><td>Format</td></tr><tr><td>1</td><td>Message descriptor</td><td>Message code</td></tr><tr><td>2</td><td>MSGLP (Note 1)</td><td>1 byte</td></tr><tr><td>3</td><td>Mapping of bearer channels to latency paths</td><td>1 byte</td></tr><tr><td>4</td><td>B_{x0}</td><td>1 byte</td></tr><tr><td>5</td><td>B_{x1}</td><td>1 byte</td></tr><tr><td>6</td><td>LP₀ (Note 2)</td><td>Latency path descriptor</td></tr><tr><td>7</td><td>LP₁</td><td>Latency path descriptor</td></tr><tr><td>8</td><td>Erasure decoding used</td><td>1 byte</td></tr><tr><td>9</td><td>Downstream SOS tone groups</td><td>Band descriptor</td></tr><tr><td>10</td><td>Downstream ROC parameters</td><td>ROC descriptor</td></tr><tr><td>11</td><td>ITU-T G.998.4 parameter field</td><td>Variable length</td></tr><tr><td>12</td><td>ITU-T G.993.5 parameter field</td><td>Variable length</td></tr></table> <p>NOTE 1 – If the ROC is enabled, MSGLP shall be equal to 0.</p> <p>NOTE 2 – If the ROC is enabled, the framing parameters for latency path #0 shall be contained in the ROC descriptor.</p> <p>...</p> <p>Field #5 "B_{x1}" is a one-byte field that indicates the number of octets from bearer channel #1 that shall be transported in each MDF in the downstream direction. The value shall be either zero or the non-zero value from the set {B₀₁, B₁₁}.</p> <p>Field #6 "LP₀" is a 10-byte field that contains the PMS-TC parameters for latency path #0 in the downstream direction. The "Latency path descriptor" format specified in Table 12-57 shall be used.</p>		Field name	Format	1	Message descriptor	Message code	2	MSGLP (Note 1)	1 byte	3	Mapping of bearer channels to latency paths	1 byte	4	B _{x0}	1 byte	5	B _{x1}	1 byte	6	LP ₀ (Note 2)	Latency path descriptor	7	LP ₁	Latency path descriptor	8	Erasure decoding used	1 byte	9	Downstream SOS tone groups	Band descriptor	10	Downstream ROC parameters	ROC descriptor	11	ITU-T G.998.4 parameter field	Variable length	12	ITU-T G.993.5 parameter field	Variable length
	Field name	Format																																						
1	Message descriptor	Message code																																						
2	MSGLP (Note 1)	1 byte																																						
3	Mapping of bearer channels to latency paths	1 byte																																						
4	B _{x0}	1 byte																																						
5	B _{x1}	1 byte																																						
6	LP ₀ (Note 2)	Latency path descriptor																																						
7	LP ₁	Latency path descriptor																																						
8	Erasure decoding used	1 byte																																						
9	Downstream SOS tone groups	Band descriptor																																						
10	Downstream ROC parameters	ROC descriptor																																						
11	ITU-T G.998.4 parameter field	Variable length																																						
12	ITU-T G.993.5 parameter field	Variable length																																						

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	<p style="text-align: center;">Table 12-57 – Latency path descriptor</p> <table><tr><th>Octet</th><th>Field</th><th>Format</th><th>Description</th></tr><tr><td>4</td><td>M</td><td>1 byte</td><td>The number of MDFs in an RS codeword for the latency path. Only the values 1, 2, 4, 8, 16 are allowable.</td></tr><tr><td>5 and 6</td><td>L</td><td>2 bytes</td><td>Contains the value of <i>L</i> for the latency path.</td></tr><tr><td>7</td><td>R</td><td>1 byte</td><td>Contains the value of <i>R</i> for the latency path.</td></tr><tr><td>8</td><td>I</td><td>1 byte</td><td>Contains the value of <i>I</i> for the latency path.</td></tr><tr><td>9 and 10</td><td>D</td><td>2 bytes</td><td>Interleaver depth <i>D</i> for the latency path.</td></tr></table> <p>Also see, e.g., ITU-T G.993.2 (02/2019) at Table 12-57:</p>	Octet	Field	Format	Description	4	M	1 byte	The number of MDFs in an RS codeword for the latency path. Only the values 1, 2, 4, 8, 16 are allowable.	5 and 6	L	2 bytes	Contains the value of <i>L</i> for the latency path.	7	R	1 byte	Contains the value of <i>R</i> for the latency path.	8	I	1 byte	Contains the value of <i>I</i> for the latency path.	9 and 10	D	2 bytes	Interleaver depth <i>D</i> for the latency path.
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4	M	1 byte	The number of MDFs in an RS codeword for the latency path. Only the values 1, 2, 4, 8, 16 are allowable.																						
5 and 6	L	2 bytes	Contains the value of <i>L</i> for the latency path.																						
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8	I	1 byte	Contains the value of <i>I</i> for the latency path.																						
9 and 10	D	2 bytes	Interleaver depth <i>D</i> for the latency path.																						
receive a flag signal, and	<p><u>ITU-T G.993.2 VDSL2 Standard</u></p> <p>The Accused Products comprises a transceiver configurable to receive a flag signal. See, e.g., ITU-T G.993.2 (12/2011) at § 3.64 Syncflag, § 10.5.3 On-line reconfiguration:</p> <p>3.64 Syncflag: A sync symbol in which the sync frame bits are inverted relative to the sync frame modulated by the most recently transmitted sync symbol (i.e., if the previous sync frame was all ZEROS, the Syncflag would correspond to a sync frame of all ONES, and vice versa). The Syncflag is used to signal online reconfiguration transitions.</p> <p>10.5.3 On-line reconfiguration</p> <p>The transmitter inserts a sync symbol every 257 symbols, as defined in clause 10.2. Therefore, a sync symbol shall be transmitted after every 256 data symbols.</p> <p>To signal on-line reconfiguration timing (see clause 13.3), the responding VTU shall send a Syncflag (see clause 3.64).</p>																								

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	See, e.g., ITU-T G.993.2 (02/2019) at § 3.64 Syncflag, § 10.5.3 On-line reconfiguration
switch to using for reception, a second FIP setting following reception of the flag signal	<p><u>ITU-T G.993.2 VDSL2 Standard</u></p> <p>The Accused Products comprises a transceiver operable to switch to using for reception, a second FIP setting. See, e.g., ITU-T G.993.2 (12/2011) at § 13.3 Timing of changes in subcarrier configuration:</p>

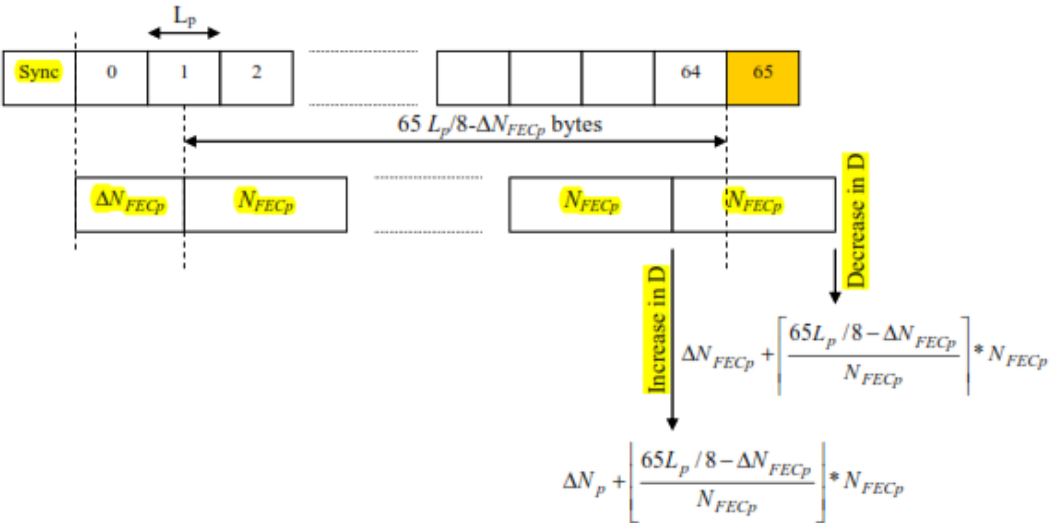
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	Table 11-6 – OLR commands sent by the initiating VTU				
	Name	Length (octets)	Octet number	Content	Support
	Request Type 1	$5 + 4 \times N_f$ ($N_f \leq 128$)	2	04 ₁₆ (Note 1)	Mandatory
			3 to 4	2 octets for the number of subcarriers N_f to be modified	
			5 to 4 + 4 × N_f	4 × N_f octets describing the subcarrier parameter field for each subcarrier	
			5 + 4 × N_f	1 octet for SC	
	Request Type 2	For further study	2	05 ₁₆ (Note 1)	For further study
			All others	Reserved by ITU-T	
	Request Type 3 (SRA) (Note 6)	$5 + 7 N_{LP} + 4 N_f$ ($N_f \leq 128$)	2	06 ₁₆ (Note 1)	Optional
			3 to 2 + 2 N_{LP}	$2 \times N_{LP}$ octets containing the new L_p values for each of the active latency paths (N_{LP} = number of active latency paths) (Notes 2 and 3)	
			3 + 2 N_{LP} to 2 + 4 N_{LP}	$2 \times N_{LP}$ octets containing the new D_p values for each of the active latency paths (N_{LP} = number of active latency paths) (Note 4)	
			3 + 4 N_{LP} to 2 + 5 N_{LP}	N_{LP} octets containing the new T_p values for each of the active latency paths (N_{LP} = number of active latency paths) (Notes 2, 3, 5)	
			3 + 5 N_{LP} to 2 + 6 N_{LP}	N_{LP} octets containing the new G_p values for each of the active latency paths (N_{LP} = number of active latency paths)	

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	<p>13.3 Timing of changes in subcarrier configuration</p> <p>In both the upstream and the downstream directions, the reconfiguration of the PMD functions shall take effect starting with the tenth symbol that follows transport of the Syncflag for OLR type 1. As defined in clause 10.2, the sync symbol is transmitted after every 256 data symbols. The reconfiguration of the PMD function shall take effect starting with the symbol at symbol count 9 in the next DMT superframe, where the first symbol in each DMT superframe is the symbol at symbol count 0.</p>

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	 <p data-bbox="554 808 1377 841">Figure 13-1 – Finding the byte where the change in D_p is activated</p> <p data-bbox="373 885 1570 1089">Figure 13-1 shows the DMT symbol counter and the byte counter at which the interleaver depth change is activated, relative to the Syncflag. For an increase in depth, the change in D_p will always happen at the same time or before the change in L_p, but as close to it as possible (i.e., the change in D_p happens during the DMT symbol with count 64 or sooner). Likewise, for a decrease in depth, the change in D_p will always happen at the same time or after the change in L_p, but as close to it as possible (i.e., the change in D_p happens during the DMT symbol with count 65 or later).</p> <p data-bbox="338 1138 1577 1170">Also see, e.g., ITU-T G.993.2 (02/2019) at § 13.3 Timing of changes in subcarrier configuration:</p>
wherein: the first FIP setting comprises at least one first FIP value,	<p data-bbox="338 1230 787 1263"><u>ITU-T G.993.2 VDSL2 Standard</u></p> <p data-bbox="338 1300 1564 1406">In the Accused Products the first FIP setting comprises at least one first FIP value, the second FIP setting comprises at least one second FIP value, different than the first FIP value See, e.g., ITU-T G.993.2 (12/2011) at § 9.4.1 Dynamic change of interleaver depth:</p>

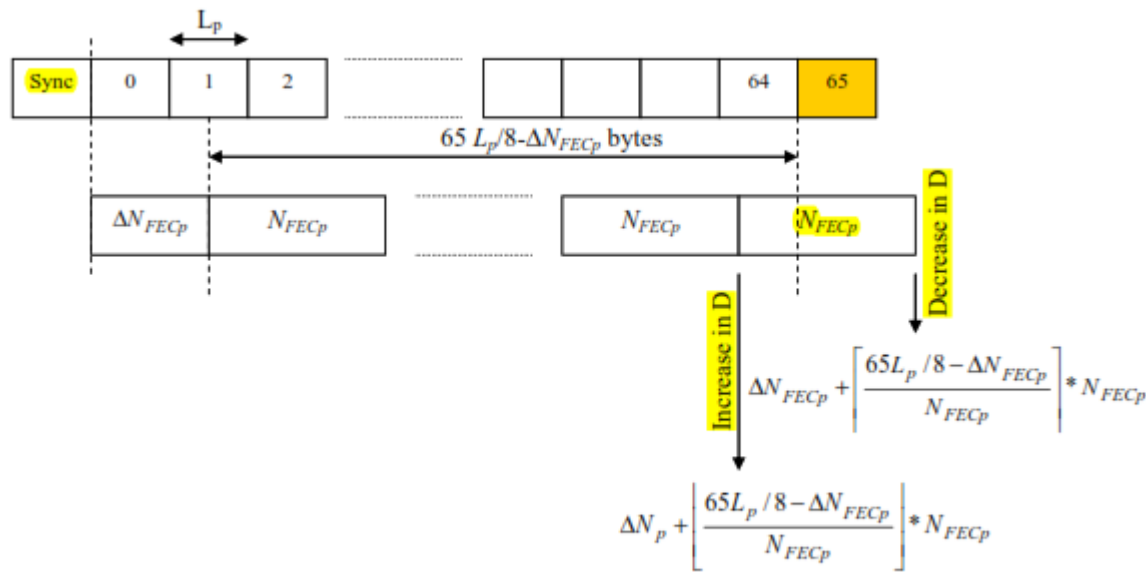
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the second FIP setting comprises at least one second FIP value, different than the first FIP value, and	<p>9.4.1 Dynamic change of interleaver depth</p> <p>A method to dynamically change the interleaver depth during transmission is defined for VDSL2. This method is optional. Support shall be indicated during initialization in O-MSG 1 and R-MSG 2.</p> <p>NOTE – Although this clause defines the procedure for dynamically changing the interleaver depth during transmission, the control command for initiating this procedure is not defined in this version of in this Recommendation. The calling procedure for dynamic change of interleaver depth will be defined in a future revision to this Recommendation.</p> <p>A change of the interleaver depth shall only be initiated at the first byte of an RS codeword, where k is the sequence number of this byte at the input of the interleaver.</p> <p>For an increase of the interleaver depth from D_{old} to D_{new} with $D_{old} < D_{new}$ the interleaver output is defined by:</p> $y(n + \Delta_{old}[j]) = x(n); \text{ for } n + \Delta_{old}(j) < k, \text{ where } \Delta_{old}[j] = (D_{old} - 1) \times j$ $y(n + \Delta_{new}[j]) = x(n); \text{ for } n + \Delta_{old}(j) \geq k, \text{ where } \Delta_{new}[j] = (D_{new} - 1) \times j$ <p>For a decrease of the interleaver depth from D_{old} to D_{new} with $D_{old} > D_{new}$ the interleaver output is defined by:</p> $y(n + \Delta_{old}[j]) = x(n); \text{ for } n + \Delta_{new}(j) + \delta < k$ $y(n + \Delta_{new}[j] + \delta) = x(n); \text{ for } n + \Delta_{new}(j) + \delta \geq k$ <p>where δ is the length of the transition and is given by:</p> $\delta = \lceil (D_{old} - D_{new}) \cdot (I - 1) / I \rceil \cdot I$ <p>Also see, e.g., ITU-T G.993.2 (02/2019) at § 9.4.1 Dynamic change of interleaver depth:</p>
the switching occurs on a pre-defined forward error correction	<p><u>ITU-T G.993.2 VDSL2 Standard</u></p> <p>In the Accused Productsthe switching occurs on a pre-defined forward error correction codeword boundary following the flag signal. See, e.g., ITU-T G.993.2 (12/2011) at § 13.3 Timing of changes in subcarrier configuration, Fig. 13-1:</p>

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codeword boundary following the flag signal.	<p>13.3 Timing of changes in subcarrier configuration</p> <p>In both the upstream and the downstream directions, the reconfiguration of the PMD functions shall take effect starting with the tenth symbol that follows transport of the Syncflag for OLR type 1. As defined in clause 10.2, the sync symbol is transmitted after every 256 data symbols. The reconfiguration of the PMD function shall take effect starting with the symbol at symbol count 9 in the next DMT superframe, where the first symbol in each DMT superframe is the symbol at symbol count 0.</p> <p>For OLR Type 3, when performed in the latency path p, the change in L_p values and b_i, g_i values shall take effect starting from the 66th symbol that follows the Syncflag, i.e., the symbol with symbol count 65 in the DMT superframe following the Syncflag, where the first symbol in the DMT superframe is the symbol at symbol count 0.</p> <p>The change of framing parameters T_p, G_p and B_{p0} shall take effect on the first OH frame of the first OH superframe that follows the 66th DMT symbol after the Syncflag.</p> <p>The change in D_p shall take effect on the first byte of an interleaved RS codeword (byte k as defined in clause 9.4.1). This codeword shall be determined as follows:</p> <ul style="list-style-type: none"> • For a decrease in interleaver depth, this shall be the first RS codeword that starts at or after the beginning of the 66th DMT symbol. • For an increase in interleaver depth, this shall be the last RS codeword that starts at or before the beginning of the 66th DMT symbol.

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	 <p style="text-align: center;">Figure 13-1 – Finding the byte where the change in D_p is activated</p> <p>See, e.g., ITU-T G.993.2 (02/2019) at § 13.3 Timing of changes in subcarrier configuration, Fig. 13-1:</p>
26. The apparatus of claim 24, wherein a first interleaver parameter value of the first FIP setting is different than a	<p><u>ITU-T G.993.2 VDSL2 Standard</u></p> <p>The Accused Products comprise an apparatus, wherein a first interleaver parameter value of the first FIP setting is different than a second interleaver parameter value of the second FIP setting. See, e.g., ITU-T G.993.2 (12/2011) at § 9.4.1, Dynamic change of interleaver depth:</p>

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second interleaver parameter value of the second FIP setting.	<p>9.4.1 Dynamic change of interleaver depth</p> <p>A method to dynamically change the interleaver depth during transmission is defined for VDSL2. This method is optional. Support shall be indicated during initialization in O-MSG 1 and R-MSG 2.</p> <p>NOTE – Although this clause defines the procedure for dynamically changing the interleaver depth during transmission, the control command for initiating this procedure is not defined in this version of in this Recommendation. The calling procedure for dynamic change of interleaver depth will be defined in a future revision to this Recommendation.</p> <p>A change of the interleaver depth shall only be initiated at the first byte of an RS codeword, where k is the sequence number of this byte at the input of the interleaver.</p> <p>For an increase of the interleaver depth from D_{old} to D_{new} with $D_{old} < D_{new}$ the interleaver output is defined by:</p> $y(n + \Delta_{old}[j]) = x(n); \text{ for } n + \Delta_{old}(j) < k, \text{ where } \Delta_{old}[j] = (D_{old} - 1) \times j$ $y(n + \Delta_{new}[j]) = x(n); \text{ for } n + \Delta_{old}(j) \geq k, \text{ where } \Delta_{new}[j] = (D_{new} - 1) \times j$ <p>For a decrease of the interleaver depth from D_{old} to D_{new} with $D_{old} > D_{new}$ the interleaver output is defined by:</p> $y(n + \Delta_{old}[j]) = x(n); \text{ for } n + \Delta_{new}(j) + \delta < k$ $y(n + \Delta_{new}[j] + \delta) = x(n); \text{ for } n + \Delta_{new}(j) + \delta \geq k$ <p>where δ is the length of the transition and is given by:</p> $\delta = \lceil (D_{old} - D_{new}) \cdot (I - 1) / I \rceil \cdot I$ <p>See also, e.g., ITU-T G.993.2 (02/2019) at § 9.4.1, Dynamic change of interleaver depth.</p>